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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/615,014	07/09/2003	Mutsumi Kimura	116029	8728

25944 7590 07/28/2004

EXAMINER
SEFER, AHMED N

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ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 07/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/615,014	KIMURA, MUTSUMI	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

~~4a) Of the above claim(s) *3 and 5-17* is/are withdrawn from consideration.~~

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/29/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election with traverse of second embodiment, Figs. 4 and 5 in the reply filed on July 2, 2004 is acknowledged. The traversal is on the ground(s) that the search and examination of the entire application could be made without serious burden. Examiner respectfully disagrees with applicant's argument and reiterates that the application includes claims to distinct species making election of a single disclosed species proper. Furthermore, since claims 5, 6, 8-11 and 17 are not readable on the second embodiment (figs. 4 and 5 do not show a switching transistor), 5, 6, 8-11 and 17 have been withdrawn.

The requirement is still deemed proper and is therefore made FINAL.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Ohori et al. ("Ohori") USPN 6,025,607.

Ohori discloses in fig. 1c a thin-film transistor, comprising: an active region; a source region; and a drain region, the source region and the drain region being provided at each side of the active region, respectively; the source region 21B and the drain region 21C including regions adjacent to the active region, the adjacent regions including lightly doped impurity regions with an impurity concentration less than an impurity concentration of the drain region; and the lightly

doped impurity regions 21F/21G being provided in an asymmetrical form in which the lightly doped impurity region 21F in the source region is smaller than the drain region or the length, in the longitudinal direction of a channel, of the lightly doped impurity region 21G in the drain region being longer than the lightly doped impurity region 21F in the source region (as in claim 2).

As for claim 4, Ohori discloses a gate electrode 22 provided at a position facing the active region, with an insulating layer provided 21a therebetween, the boundary between each lightly doped impurity region and the active region approximately matching one end of the gate electrode.

4. Claims 1, 2 and 4 are rejected under 35 U.S.C. 102(b) as being anticipated by Shibuya et al. ("Shibuya") USPN 6,078,060.

Shibuya discloses in fig. 3B a thin-film transistor, comprising: an active region; a source region 111; and a drain region 113, the source region and the drain region being provided at each side of the active region, respectively; the source region and the drain region including regions adjacent to the active region, the adjacent regions including lightly doped impurity regions 128/130 with an impurity concentration less than an impurity concentration of the drain region; and the lightly doped impurity regions being provided in an asymmetrical form in which the lightly doped impurity region 128 in the source region is smaller than the drain region or the length, in the longitudinal direction of a channel, of the lightly doped impurity region 21G in the drain region being longer than the lightly doped impurity region 130 in the source region (as in claim 2).

As for claim 4, Shibuya discloses a gate electrode 122 provided at a position facing the active region, with an insulating layer provided therebetween, the boundary between each lightly doped impurity region and the active region approximately matching one end of the gate

5. Claims 1 and 2 are rejected under 35 U.S.C. 102(b) as being anticipated by Kunii US PG-Pub 2002/0068372.

Kunii discloses in fig. 8H a thin-film transistor, comprising: an active region; a source region; and a drain region, the source region and the drain region being provided at each side of the active region, respectively; the source region S and the drain region D including regions adjacent to the active region, the adjacent regions including lightly doped impurity regions with an impurity concentration less than an impurity concentration of the drain region; and the lightly doped impurity regions being provided in an asymmetrical form in which the lightly doped impurity region in the source region is smaller than the drain region (high impurity S/D region shares space with LDD portion of the source region which results in smaller LDD portion on the source side) drain region or the length, in the longitudinal direction of a channel, of the lightly doped impurity region 21G in the drain region being longer than the lightly doped impurity region 21 F in the source region (as in claim 2).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANS
July 25, 2004

Minhloan Tran
Primary Examiner
Art Unit 2826